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LGE VS [OEM Name] [Project Name]

**System Architectural Design**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **About This Template**   * Template title: LGE\_VS\_SysAD\_T01\_System Architectural Design (SysAD) * Management Department: VS SW Process Team * Revision History  |  |  |  |  |  | | --- | --- | --- | --- | --- | | Version | Date | Comment | Author | Approver | | 1.5 | 2016-09-30 | Initial Release | VC SW Process Team  CTO SEL | VC Smart QE FD | | 1.6 | 2019-02-19 | Update due to annual organization restructuring (VC 🡪 VS) | VC Smart SW Process team | VS Smart SW Process team | | 2.1 | 2021-08-23 | (\* actually updated in 19.02.21 by Guawnrok Park, Architec team)  Updated overall   * Contents * Document structure | VC Smart SW Process Unit | VC Smart SW Process Unit Leader | | Updated security notice of this template  (Before: LGE Confidential->After: LGE Internal Use Only) Security level related note (the last sentence in red color below) |  * Blue fonts is just an example for reference. * The contents of this template may not be 100% right for all projects, so authors should use it after tailoring the contents to the project characteristics. * Once you have finished this document, delete "About This Template" part. * The notice “LGE Internal Use Only” is for this template itself. The document which use this template needs to be classified as suitable security level according to its content |

About This Document

Document Information

|  |  |
| --- | --- |
| Issuing authority | VS OOO Team |
| Configuration ID | Configuration Item ID in CMBook |
| **Status of document** | In progress / Approved / Released |

Revision History

|  |
| --- |
| Sort the revision history from newest to oldest. |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Verion | Date | Comment | Author | Approver |
| #.# | YYYY-MM-DD | OOOOOOOOOOOOOOO | OOO | OOO |
| 1.1 | 2016-02-20 | Modified xxx notation of C&C Diagram in 2.2 C&C View. | Gildong Hong | Sam Shin |
| 1.0 | 2016-01-20 | Initial Release | Gildong Hong | Sam Shin |

Table of Contents

|  |
| --- |
| Table of contents is automatically created if you use [field update] feature of Microsoft Word. |

[1 Introduction 7](#_Toc533077133)

[1.1 Purpose 7](#_Toc533077134)

[1.2 Scope 7](#_Toc533077135)

[1.3 Audience 7](#_Toc533077136)

[1.4 Conventions 7](#_Toc533077137)

[1.5 Acronyms / Glossary 8](#_Toc533077138)

[1.6 Related Documents 8](#_Toc533077139)

[2 Architectural Drivers 9](#_Toc533077140)

[2.1 Major Functionality 9](#_Toc533077141)

[2.2 Major Quality Attribute 9](#_Toc533077142)

[2.3 Constraints 10](#_Toc533077143)

[3 System Context 11](#_Toc533077144)

[3.1 External Interface Specification 11](#_Toc533077145)

[4 System Architecture 12](#_Toc533077146)

[4.1 Physical View of the System Architecture 12](#_Toc533077147)

[4.2 System Elements Specification 13](#_Toc533077148)

[4.3 System Internal Interface Specification 14](#_Toc533077149)

[5 Mechanic Design / Connector 15](#_Toc533077150)

[5.1 Mechanic Design 15](#_Toc533077151)

[5.1.1 System Dimension 15](#_Toc533077152)

[5.1.2 Mechanic Configuration 15](#_Toc533077153)

[5.1.3 Installation interface 16](#_Toc533077154)

[5.2 System Connectors 17](#_Toc533077155)

[5.2.1 Connector name #1 (External IF\_ID: E0X) 17](#_Toc533077156)

[5.2.2 Connector name #n (External IF\_ID: E0X) 17](#_Toc533077157)

[6 Dynamic Design 18](#_Toc533077158)

[6.1 Power Mechanism 18](#_Toc533077159)

[6.2 Diagnosis Mechanism 20](#_Toc533077160)

[6.3 Calibration mechanism 21](#_Toc533077161)

[6.4 Watchdog Mechanism 21](#_Toc533077162)

[6.5 Configuration Mechanism 21](#_Toc533077163)

[7 Functional Safety Mechanism 22](#_Toc533077164)

[7.1 Safety Architecture 22](#_Toc533077165)

[7.2 Safety Function List 22](#_Toc533077166)

[7.3 Safety Function Details 23](#_Toc533077167)

[8 QA Scenario Analysis / Design Alternatives 24](#_Toc533077168)

[8.1 QA Scenario#1 24](#_Toc533077169)

[8.2 QA Scenario#2 25](#_Toc533077170)

[8.3 Reflectivity 25](#_Toc533077171)

[9 HW-SW Interfaces 26](#_Toc533077172)

Figures

|  |
| --- |
| Table of contents is automatically created if you use [field update] feature of Microsoft Word. |

[Figure 3.1 System Context 11](#_Toc533077173)

[Figure 4.1 Physical View of the System Architecture 12](#_Toc533077174)

[Figure 5.1 System Appearance & dimension 15](#_Toc533077175)

[Figure 5.2 Mechanic Configuration 15](#_Toc533077176)

[Figure 5.3 Interface for installation 16](#_Toc533077177)

[Figure 5.4 Connector name layout 17](#_Toc533077178)

[Figure 6.1 shows power mode process after Batter power supply. 19](#_Toc533077179)

[Figure 6.2 Power mode process sample 19](#_Toc533077180)

[Figure 7.1 Safety Architecture 22](#_Toc533077181)

Tables

|  |
| --- |
| Table of contents is automatically created if you use [field update] feature of Microsoft Word. |

[Table 1.1 System Objective 7](#_Toc533077182)

[Table 2.1 Feature List 9](#_Toc533077183)

[Table 3.1 System External Interfaces 11](#_Toc533077184)

[Table 4.1 System Elements Specifications 13](#_Toc533077185)

[Table 4.2 System Internal Interface Specification 14](#_Toc533077186)

[Table 5.1 Pin Assignment for Connector name 17](#_Toc533077187)

[Table 6.1 Power Mode table 18](#_Toc533077188)

[Table 6.2 DTC List 20](#_Toc533077189)

[Table 7.7.1 Safety Function List 22](#_Toc533077190)

[Table 7.2 System level Safety Mechanism 23](#_Toc533077191)

# Introduction

## Purpose

|  |
| --- |
| Describe the purpose of this document. |

This document specifies the System Requirements Specifications for XXX.

Table 1.1 System Objective

|  |  |
| --- | --- |
| System name |  |
| Purpose of the system in vehicle | *Describe the purpose and brief functionality of the system in the view point of vehicle function* |

*[Use the Customer requirements and stakeholder requirements to create system requiements spec. (informative)]*

## Scope

|  |
| --- |
| Describe the scope of this document. |

* Scope covered by this document:
* Scope of this document (OEM/model/country):
* Scope of development / undeveloped scope of this project:

## Audience

|  |
| --- |
| Describe the audiences of this document. |

The target audience of this document is:

* Requirement engineer who will point out any contradiction between the design and the requirement
* System / Software architect who will evaluate the design of the system / software
* Component developer who will implement the design in actual code
* XXX project participants who want to understand the architecture of the [System Name]
* Test engineers who verify [System Name] and others related

## Conventions

|  |
| --- |
| If there is a notation used in this document, explain it. |

Example 1: unit of measure

**Units**

The unit of speed keeps consistency for each destination.

Japan: km/h

U.S.: mile/h

Example 2: This document follows UML notation 2.0

## Acronyms / Glossary

|  |
| --- |
| Describes abbreviations used in this document and their interpretations. In the table, the abbreviations/terms are indicated in alphabetical order. In addition to explaining abbreviations, it is written when explanations of terms are required. |

|  |  |
| --- | --- |
| Acronym | Description |
| CAN | Controller Area Network |
| DD | Download Descriptor |
| ERR | External Remote Reflash |
| IRR | Internal Remote Reflash |
| LIN | Local Interconnect Network |
| SysAD | System Architectural Design |
| SysRS | System Requirements Specifications |

|  |  |
| --- | --- |
| Glossary | Description |
| Feature | A set of related functions |
|  |  |

## Related Documents

|  |
| --- |
| Describe the list of documents referenced when preparing this document. |

Documents related to this document include:

[1] LGE, Customer Requirements Specifications, pjt\_CRS, v1.0[, Date][, Page]

[2] LGE, System Requirements Specifications, pjt\_SyRS\_feature, v1.0[, Date][, Page]

[3] Author, Document title, Document version [Date] [Page]

Documents referenced from this document include:

[11] LGE, SyAD template, pjt\_SyAD (LGE VC SyRS tpl v2.0), 2017.6.10

# Architectural Drivers

< This chapter/section describes the main factors that determine the system architecture. >

## Major Functionality

*[■ Contents: Describe system main features or use case diagrams as below table.]*

Table 2.1 Feature List

|  |  |  |
| --- | --- | --- |
| No | Function name | UC\_ID |
| *1* | *Battery Performance Estimation* |  |
| *2* | *Thermal Control* |  |
| *3* | *Cell Balancing Control* |  |
|  |  |  |
|  |  |  |
|  |  |  |

## Major Quality Attribute

< Among the system quality attribute requirements of SysRS, the major quality attributes required for the system are selected, and the Quality Attribute Scenario and priority are determined for each quality attribute. The design and design decisions for this are described in Chapter 8.>

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QA type** | **Quality Attribute Scenario** | | | | **Priority** |
| Reflectivity | CSD need to archive readability with incident sunlight.  Reflectivity must be less than 1%. (SyRS ID : S.Pxx) | | | | High |
| **Source** | **Stimulus** | **Artifacts** | **Environment** | **Response** | **Measure** |
| Sun | Sunlight | Display | Day Light | Reflectivity | <1% |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **QA type** | **Quality Attribute Scenario** | | | | **Priority** |
| Luminance | Display shall be designed to achieve luminance 600cd/m².  (SyRS ID : S.P031) | | | | High |
| **Source** | **Stimulus** | **Artifacts** | **Environment** | **Response** | **Measure** |
| BLU | Backlight | Display | Temperature | Luminance | > 600cd/m² |

## Constraints

< Among the Design Constraints described in SysRS, major items related to the system structure are selected. >

1. *Operating temperature, humidity*
2. *Specification for installation*
3. *Target weight of the system (incl. protection case)*
4. *Specification for power*
5. *Allowed power consumption*
6. *Allowed current leakage (dark current)*
7. *Max CPU, MEM, ROM occupation rate*
8. …

# System Context

*[■ Draw the relationship between this system and an entity outside the system and briefly explain it. Assign external interface ID and describe it in a table.]*

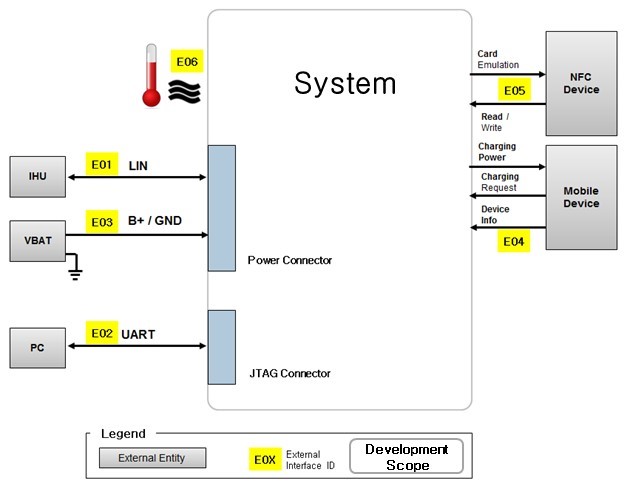


Figure 3.1 System Context

## External Interface Specification

Table 3.1 System External Interfaces

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Ext\_IF\_ID | IF\_Name | External element name | Connector Spec. | Specification for interface | SyRS\_ID |
| *E01* |  | *CMC* | *CON\_2: A3* | *BMS should receive "alarm" signal from CMC by using hardwired connection*  *- Active High (4.75V ~ 4.95V)*  *BMS should be able to detect circuit-open of the connection* |  |
| E02 |  |  |  |  |  |
|  |  |  |  |  |  |

[■ ‘Specification for interface’ includes communication specifications.]

# System Architecture

## Physical View of the System Architecture

*[■ Contents: Identify the system elements on the system structure diagram and describe the internal interface between them. Assign IDs to system elements and internal interfaces, and add legends. (SysML, UML, Simulink, or equivalent level of notation is recommended)]*

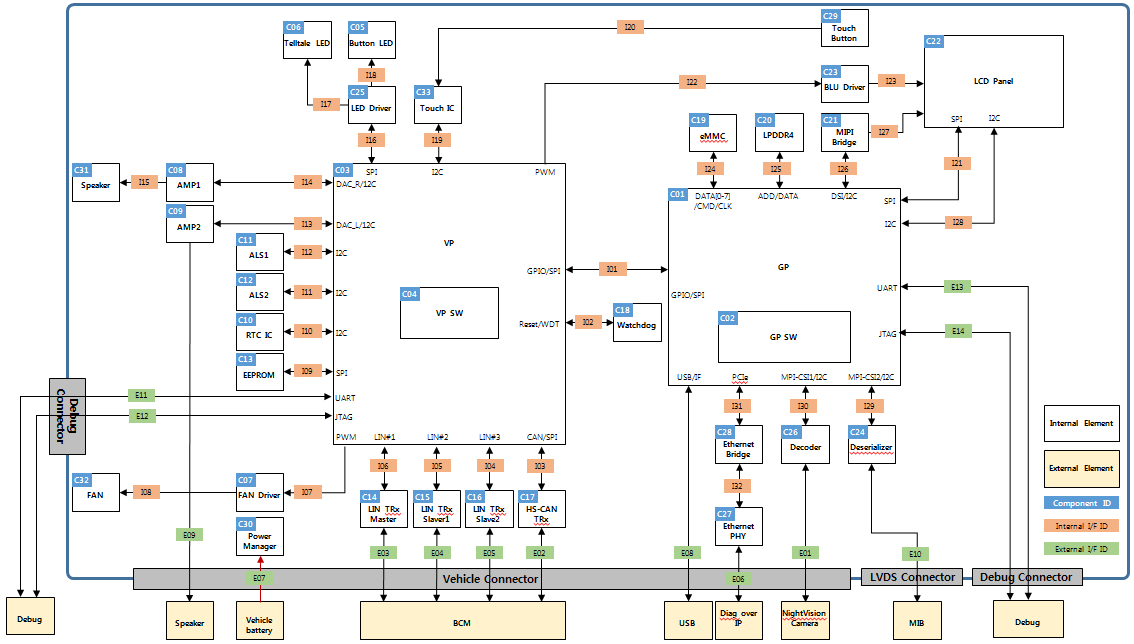


Figure 4.1 Physical View of the System Architecture

<System architecture is briefly described.>

## System Elements Specification

*[■ Contents: Define specifications for each system element identified in Fig4.1 considering the characteristics.*

*: Memory specification (e.g. required code area size, data area size / memory cycle speed / etc.)*

*: Hardware interface between elements (e.g. SPI, I2C, Address/Data access, Hardwired, etc.)*

*: User interface (if applicable) (e.g. Display specification of warning message)*

*: Security and data protection*

*: Parameter setting (e.g. Gain value)*

*: Dependency between elements*

*: Reusable component or not*

*: Logical behavior on element level (not system level)*

*: Performance specification]*

Table 4.1 System Elements Specifications

|  |  |  |  |
| --- | --- | --- | --- |
| System element ID | System element name | Specification (\*Note) | SyRS\_ID |
| *C01* | *External ADC* | *ADC should be controlled by MCU via SPI communication interface.*  *ADC should be able to measure 0V to xxV in minimum resolution of 1.5%* | *SyRS.63* |
| *C02* |  |  |  |
| *C03* |  |  |  |
|  |  |  |  |

## System Internal Interface Specification

*[■ Contents: Items below should be included when you describe the specifications for each internal interface identified in Fig 4.1.*

*: HW interface mechanism*

*: Allowed communication latency*

*: Signal/message protection method*

*: Signal/message validation method*

*: Signal/message priority*

*: Signal/message sequence]*

Table 4.2 System Internal Interface Specification

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Interface ID | Element ID  (From) | Element ID  (To) | Interface Type | Specifications | SyRS\_ID |
| *I01* | *(SYS-EL-04)*  *MCU* | *(SYS-EL-03)*  *External ADC* | *SPI* | *Message sender should send message count in the payload frame.*  *Message count value should be increased by each sender.* | *SyRS.52* |
| *I02* | *(SYS-EL-05)*  *HSD* | *(SYS-EL-04)*  *MCU* | *DIO* | *On/Off status of the relay in HSD should be fed to DIO of MCU* | *SyRS.48* |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

# Mechanic Design / Connector

## Mechanic Design

### System Dimension

*[■ Contents: Describe mechanic design and high level dimension of system.]*

|  |  |
| --- | --- |
|  |  |
| **<3D appearance>** | **<2D appearance>** |

Figure 5.1 System Appearance & dimension

### Mechanic Configuration

*[■ Contents: Describe mechanic configuration and part list.]*

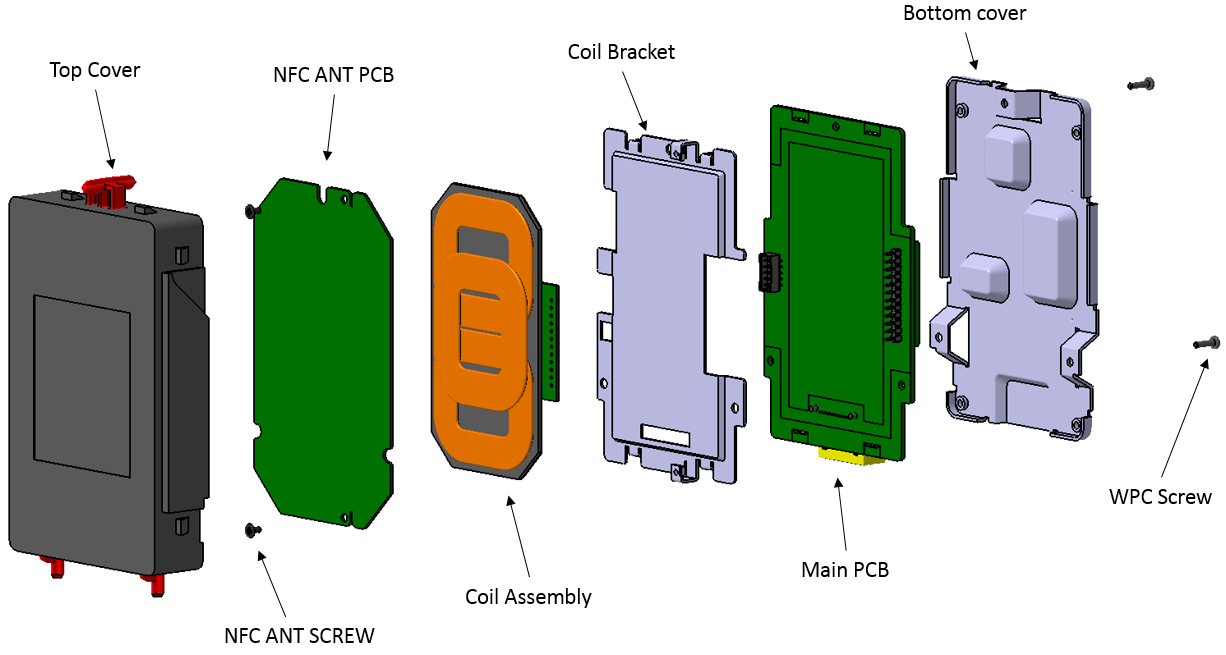


Figure 5.2 Mechanic Configuration

Table 5.1 Mechanic Part list

|  |  |  |  |
| --- | --- | --- | --- |
| ME\_ID | Item | Material / Spec. | Weight |
| ME01 | Top Case | PC+ABS | 20g |
| ME02 | NFC antenna PCB | FR4 1T | 15g |
| … |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
| Total | | | 200g |

### Installation interface

*[■ Contents: Describe the structure where the system is installed and interface of vehicle.]*

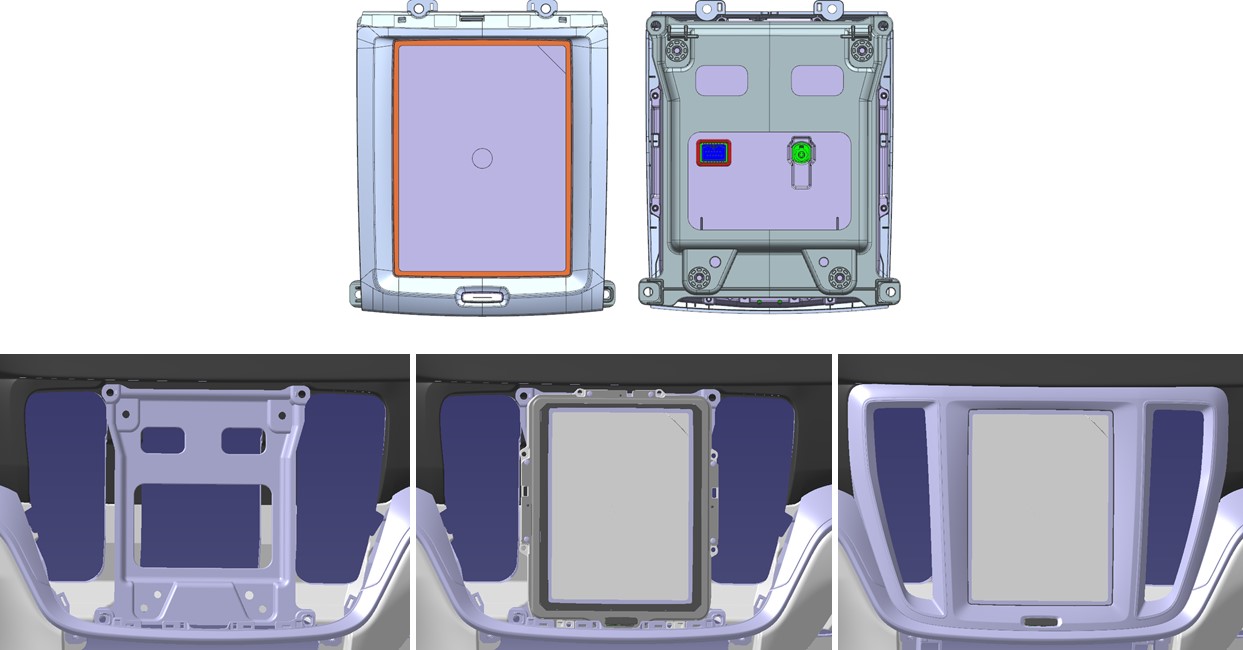


Figure 5.3 Interface for installation

## System Connectors

### Connector name #1 (External IF\_ID: E0X)

*[■ Contents: Connector and Pin location]*

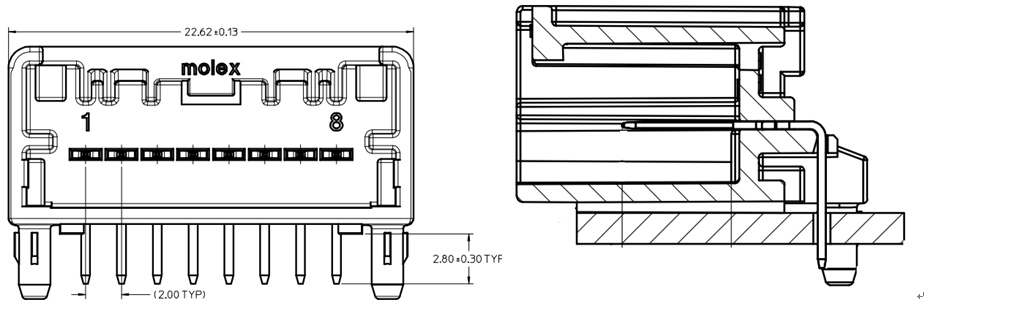


Figure 5.4 Connector name layout

*[■ Contents: Connector identifier, Pin number, Pin name (signal name), Pin interface type, Range of phisical valid value]*

Table 5.1 Pin Assignment for Connector name

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| IF\_ID | Pin No. | Pin Name | IF Type | Description | Signal Range |
| *E01* | *A1* | *B+* | *Hard-wired Power line* | *BAT power line* | *0 ~ 14.6V* |
| *E01* | *A2* | *GND* | *Hard-wired Power line* | *BAT power line* | *0 ~ 14.6V* |
| *E02* | *...* | *T1 Sensor* | *ADC* | *Temp sensor* |  |
| *E02* | *…* | *LED* | *PWM* | *Power Level indicator* | *0 ~ 100%* |
|  |  |  |  |  |  |

### Connector name #n (External IF\_ID: E0X)

# Dynamic Design

< The operating mechanism (Dynamic view) of the main functions provided by the system to the vehicle is described by dividing it into sub-sections.

NOTE 2: Dynamic behavior is determined by operating modes (e.g. start-up, shutdown, normal mode, calibration, diagnosis, etc.)[11]. >

## Power Mechanism

*[■* Contents: Draw the power sequence and present the operation sequence for each system state transition as a flowchart*]*

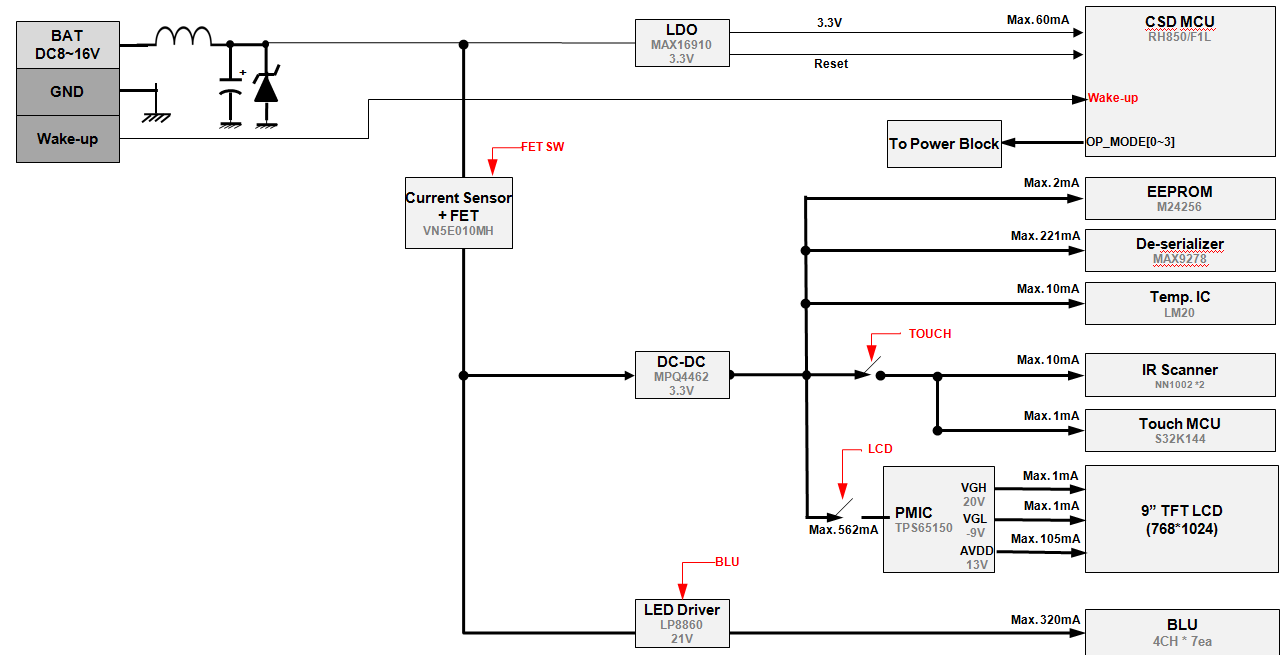


Figure 6.1 Power Sequence sample

Power operation mode is as Table 6.1.

Table 6.1 Power Mode table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| OP Mode | CSD MCU | Control Status | | | | Current |
| FET SW | Touch Block | LCD Block | BLU Block |
| **Sleep** | On | Off | NA | NA | NA | <100uA |
| **Touch** | On | On | On | Off | Off | <200mA |
| **Normal** | On | On | On | On | On | <2,000mA |

Figure 6.1 shows power mode process after Batter power supply.

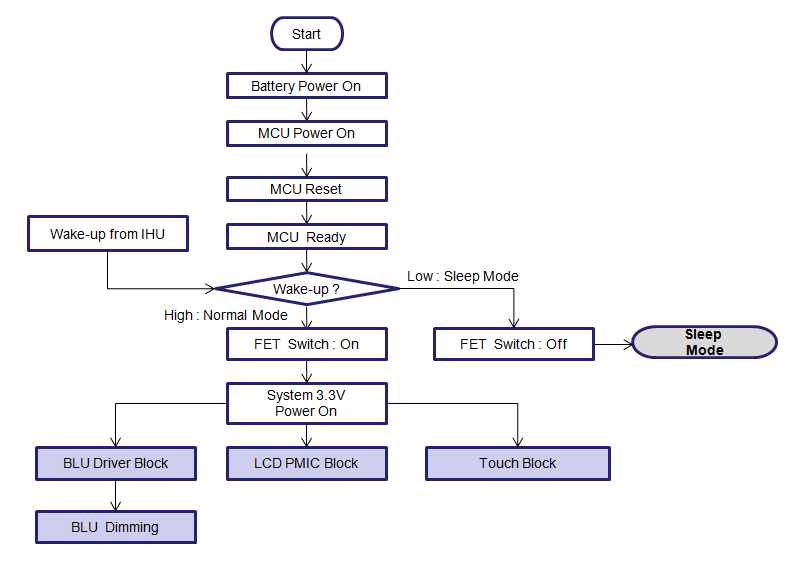


Figure 6.2 Power mode process sample

## Diagnosis Mechanism

*[■ Contents: Describe diagnosis mechanism and relevant diagnosis communication protocol, data, interface, etc.]*

Figure 6.3 Diagnosis Mechanism

Table 6.2 DTC List

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| No | DTC | Fault name | Diag. condition | Diag. interval | Reaction | Recovery condition | Allowed recovery latency |
| *1* | *C1101* | *BMS internal RAM check error* | *BMS is in running mode* | x ms | *Step1: SW reset x times*  *Step2: HW reset 1 time (fail to recover from step2)*  *Step3: Battery disconnected by external watch-dog (fail to recover from step2)* | *"OK" is detected after full-diagnosis in next vehicle driving cycle* |  |
| *2* | *C1102* | *Cell voltage plausibility check fail* |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

## Calibration mechanism

< Defines calibration mechanism of the system.

- Calibration parameter list

- Specification for each calibration parameter

- Representative calibration parameter value for each vehicle model variants >

## Watchdog Mechanism

< Defines watchdog mechanism of the system.

- Master slave

- time out & Reset

- stop and restart >

## Configuration Mechanism

# Functional Safety Mechanism

[■ Note: It can be omitted in projects that do not perform ISO 26262 (Functional Safety).

Functional safety related contents can be composed of separate documents.]

## Safety Architecture

*[■ Contents: Describe the safety architecture to explain the operation of the safety function in 7.2. The following should be considered.*

*: Marking of system elements related to the performance of each safety function*

*: Interaction between system elements related to the operation of each safety function (control signals and data)]*

|  |
| --- |
|  |

Figure 7.1 Safety Architecture

## Safety Function List

Table 7.7.1 Safety Function List

|  |  |  |
| --- | --- | --- |
| ID | Safety function name | SyRS\_ID |
| *SF01* | *Battery Management Function (BMF) Monitor* |  |
| *SF02* | *Safety Memory Monitor* |  |
| *SF03* | *Safety Fault Reaction* |  |
|  |  |  |

## Safety Function Details

*[■ Contents: Describe the details of each safety function considering the following items*

*: The type of defect to be detected (e.g. signal drift, line-off, short to VCC, etc.)*

*: A method for detecting the defect*

*: When the corresponding fault is detected, the system responds*

*: Time constraint to satisfy FTTI*

*: Whether it is related to DTC, etc.]*

*<List-up system-level safety mechanisms and explain each safety mechanism. >*

Table 7.2 System level Safety Mechanism

|  |  |  |
| --- | --- | --- |
| Safety Mechanism | Description | Related TSR  (SyRS\_ID) |
| System-level safety mechanism | *Explain the safety mechanism :*  *(If necessary, use semi-formal techniques such as activity diagrams)*  *Detection Target :*  *Detection Method :*  *System Reaction :*  *Time Constraints :*  *DTC :* | Technical safety requirement Identifier(SyRS\_ID) |
| SM01 *Monitor the BMS* | *Detection Target : Program flow corruption in BMF*  *Detection Method :*  *1. Control sequence monitor*  *- Check the control sequence of BMF based on static control flow according to BSM operation mode*  *2. Battery disconnection actuator control monitor*  *- Decide the required "battery disconnection switching" based on following information*  *-- Pack voltage, alarm signal from CMC and F/B from battery disconnection actuator*  *System Reaction :*  *Step1*  *- Send "disconnection" signal to BMF from safety function layer*  *- Send "BMS failure message" to HCU*  *Step2 (in case of function fail in step1)*  *- Disconnect "high side power path control" and "low side power path control" by disable switch#1 and switch#2*  *Time Constraints :*  *- Step1 should be completed in xx ms*  *- Failure confirmation should be executed in 5 time in succession in xx ms*  *DTC : 0x5F* | *TSR 10, 12, 52* |

# QA Scenario Analysis / Design Alternatives

< Analyze the major quality attributes defined in Chapter 2, and analyze design alternatives and decisions, risks, and trade-offs. >

## QA Scenario#1

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **QA Type** | **Quality Attribute Scenario** | | | | | | | | | | **Priority** | |
| QA type | Describe the scenario (SyRS\_ID) | | | | | | | | | | High | |
| Business Goal | Describe the business goals that are affected by the scenario | | | | | | | | | | | |
| **Source** | **Stimulus** | | **Artifacts** | | | **Environment** | | | **Response** | | **Measure** | |
| The entity that generated the stimulus | The condition that affects the system | | The artifact that was stimulated | | | The condition under which the stimulus occurred | | | The activity that results from the stimulus | | The measure by which the system’s response will be evaluated | |
| Architectural Decisions and Reasoning | List design alternatives.  Alternative #1: …  Alternative #2: …  Choice : #1  Rationale : Describe the architectural decisions relevant to this scenario that affect quality attribute response and a discussion of the qualitative and/or quantitative rationale for why the architectural decisions contribute to meeting the quality attribute response requirement | | | | | | | | | | | |
| Trade-off  Analysis | Alternative | time to market | | Cost | Risk | | System qualities | Reuse | | Use proven technologies | | Performance | |
| #1 | **Yes** | | **Yes** | No | | NO | **Yes** | | Unknown | | No | |
| #2 | No | | No | **Yes** | | **Yes** | Unknown | | Yes | | Unknown | |

<The proposed alternatives are illustrated with pictures, but the determined alternatives must be included.>

## QA Scenario#2

## Reflectivity

# HW-SW Interfaces

For the part where HW-SW interface occurs among the system internal interfaces, it is the scope of the system integration test, so it is specified so that it can be tested.

<It can be written as a separate document>

Table 9.1 HSI Table

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Hardware | | | | | | | Software | | | |
| IF\_ID | Sys Element | PIN\_name | Signal Name | Signal type | Signal Value/ Range | VC | Register name | SW Variable Name | SW Initial Value | Description |
|  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |
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